IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) :	Mahmoud A. Mousa	Group Art Unit: 2822
Appln. No. :	10/711,167	Examiner: CHIU, Tsz K.
Filed :	August 30, 2004	Confirmation No.: 5166
For :	MULTILAYER SILICON OVER INSULATOR DEVICE	

AMENDMENT UNDER 37 CFR 1.111

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In response to the Office Action dated March 1, 2006, please amend the above-identified application as follows.

A listing of claims is set forth on pages 2-4.

Remarks begin on page 5.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. 09-0456.

AMENDMENT TO THE CLAIMS

Please **ADD** claims 21-24 as follows.

A copy of all pending claims and a status of the claims are provided below.

1-13 (canceled)

14. (original) A circuit, comprising:

a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation; and

an upper semiconductor device having an active region comprising a semiconductor with a second crystal orientation, wherein the upper semiconductor device is formed separately from the lower semiconductor device and connected thereto by an interconnect structure.

15. (original) The circuit of claim 14, wherein the first crystal orientation is different from the second crystal orientation.

16. (original) The circuit of claim 14, further comprising at least one layer of a semiconductor device between the lower and upper semiconductor devices.

17. (original) The circuit of claim 16, wherein at least one semiconductor device of the at least one layer of semiconductor device comprises an active region

having a crystal orientation different from the crystal orientation of at least any one of the lower semiconductor device and the upper semiconductor device.

18. (original) The circuit of claim 14, wherein the upper semiconductor device is bonded to the top of the lower semiconductor device with an insulating layer, and wherein at least a portion of the upper semiconductor device is electrically connected to at least a portion of the lower semiconductor device.

19. (original) The circuit of claim 18, wherein:

the lower semiconductor device includes either a pFET device or an nFET device, and the upper semiconductor device includes either a pFET device or an nFET device; and

the crystal orientation of the active region of the respective lower semiconductor device is different from the crystal orientation of the active region of the respective upper semiconductor device.

20. (original) The circuit of claim 18, wherein the lower and upper semiconductor devices comprise an inverter, and the pFET device has a crystal orientation of [100] in an active region and the nFET device has a crystal orientation of [110] in an active region.

21. (new) The circuit of claim 18, further comprising a gate oxide formed on a top of the active region of the upper semiconductor device.

22. (new) The circuit of claim 21, further comprising a poly gate formed on top of the gate oxide, with an upper poly contact to voltage bus.

23. (new) The circuit of claim 22, further comprising metal contacts connecting to inputs of the upper semiconductor device.

24. (new) The circuit of claim 23, further comprising a lower poly contact connecting to the voltage bus.

REMARKS

Claims 14-24 are currently pending in the application. By this amendment, claims 21-24 are added for the Examiner's consideration. The above added claims do not add new matter to the application and are fully supported by the specification. For example, support for the added claims is provided in Figure 1 of the specification and the description thereof. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

35 U.S.C. §102 Rejection

Claim 14 was rejected under 35 U.S.C. §102(e) for being anticipated by U.S. Publication No. 2004/0144979 to Bhattacharyya (USPN 6,808,971). This rejection is respectfully traversed.

To reject a claim under 35 U.S.C. §102, a single reference must show all of the features of the claimed invention. The Examiner is of the opinion that Bhattacharyya shows all of the features of claim 14. Applicants respectfully disagree with the Examiner, as discussed in more detail below.

Claim 14 recites, in part

> ... a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation; and
>
> an upper semiconductor device having an active region comprising a semiconductor with a second crystal orientation, wherein the upper semiconductor device is formed separately from the lower semiconductor device and connected thereto by an interconnect structure.

However, these features are not disclosed in Bhattacharyya. More particularly, Bhattacharyya does not disclose an active region of a lower semiconductor device with a first crystal orientation and an active region of an upper semiconductor device with a second crystal orientation, different than the first crystal orientation. Instead, Bhattacharyya shows a structure with two semiconductor layers with different stress

concentrations. There simply is no mention that the semiconductor layers have different crystal orientations, which is distinguishable from stress concentrations.

More specifically, Bhattacharyya shows a CMOS inverter construction. This construction shows two device layers, a lower device 100 and an upper device 50. (See, FIG. 11.) Both of these devices are formed in the same manner, but with different stresses/strain features; that is, the semiconductor device has first layer with a relaxed crystalline lattice of silicon and germanium and a second layer with a strained crystalline lattice of silicon and germanium. The second layer is between the first layer and a transistor gate of the device. (See, col. 4, lines 14-20.) Bhattacharyya further discloses forming small voids (nanovoids) and small crystals in islands 18 by ion implanting helium 22 into material 16 and subsequently exposing material 16 to laser-emitted electromagnetic radiation which, in turn, aids in crystallization and stress relief within the material 16 during exposure to the electromagnetic radiation. (See, FIGS. 4-6.)

More specifically, Bhattacharyya discloses, for example, at col. 10, lines 3-29:

> The transistor structure 50 of FIG. 8 corresponds to an n-type field effect transistor (NFET), and in such construction it can be advantageous to have strained crystalline material 40 consist of a strained silicon material having appropriate dopants therein. The strained silicon material can improve mobility of electrons through channel region 56, which can improve performance of the NFET device relative to a device lacking the strained silicon lattice. Although it can be preferred that strained lattice material 40 comprise silicon in an NFET device, it is to be understood that the strained lattice can also comprise other semiconductive materials. A strained silicon lattice can be formed by various methods. For instance, strained silicon could be developed by various means and lattice 40 could be created by lattice mismatch with other materials or by geometric conformal lattice straining on another substrate (mechanical stress).

At col. 12, lines 49-61, Bhattacharyya further discloses:

> Layers 26 and 40 can correspond to a relaxed crystalline lattice material and a strained crystalline lattice material, respectively, as discussed previously with reference to FIGS. 2-8. The material 26 can comprise, consist essentially of, or consist of appropriately doped silicon/germanium; and the layer 40 can comprise, consist essentially of, or consist of appropriately doped silicon, or can comprise, consist essentially of, or consist of appropriately doped silicon/germanium.
>
> Layers 16, 26 and 40 can be considered to be crystalline layers supported over substrate 104. In particular aspects, all of layers 16, 26 and 40 are crystalline, and can be considered to together define a crystalline structure.

However, it is well known that by using these materials, the underlying layer can be placed in stress or strain, depending on whether an N-type or P-type device is to be fabricated. (See, for example, the background of Bhattacharyya.) However, Bhattacharyya does not disclose that the orientation of the crystalline structure is different for each layer, even though ample opportunity was provided.

Additionally, as disclosed at col. 8, lines 7-17 and 59-65,

> ... semiconductive material 26 has been transformed into a crystalline material (illustrated diagrammatically by the cross-hatching of material 26 in FIG. 6). Crystalline material 26 can consist of a single large crystal, and accordingly can be monocrystalline. Alternatively, crystalline material 26 can be polycrystalline. If crystalline material 26 is polycrystalline, the crystals of the material will preferably be equal in size or larger than the blocks 18. In particular aspects, each crystal of the polycrystalline material can be about as large as one of the shown islands 18.
>
> Strained lattice layer 40 can be large polycrystalline or monocrystalline. If strained lattice layer 40 is polycrystalline, the crystals of layer 40 can be large and in a one-to-one relationship with the large crystals of a polycrystalline relaxed crystalline layer 26. Strained lattice layer 40 is preferably monocrystalline over the individual blocks 18.

These passages clearly stand for the proposition that the crystalline material 26 can be monocrystalline or polycrystalline; however, these passages, which clearly describe the

crystal structure do not mention, in any way whatsoever, the orientation of the crystals. This same or similar description is provided throughout the disclosure of Bhattacharyya such as, for example, at col. 9.

Thus, it is clear from a fair reading of the Bhattacharyya disclosure, that Bhattacharyya does not contemplate different crystal orientations to provide for increased device characteristics. Instead, Bhattacharyya shows using different stress strain states of the material to provide for increased device characteristics.

Accordingly, Applicants respectfully request that the rejection over claim 14 be withdrawn.

35 U.S.C. §103 Rejection

Claims 15-20 were rejected under 35 U.S.C. §103(a) for being unpatentable over Bhattacharyya in view of U. S. Patent No. 5,384,473 to Yoshikawa. This rejection is respectfully traversed.

Claims 15-20 are dependent claims, depending from a distinguishable independent claim. Accordingly, claims 15-20 are also distinguishable and are in condition from allowance. Accordingly, Applicants respectfully request that the rejection over claims 15-20 be withdrawn.

The dependent claims also stand on their own merits, as being allowable. For example, claim 17 recites that the layer between the two devices has a crystal orientation different from the crystal orientation of at least any one of the lower semiconductor device and the upper semiconductor device. The Examiner is of the opinion that this feature is shown in Bhattacharyya. Applicants note that Bhattacharyya shows layers with different stress/strain contents, but does not disclose layers with different crystal orientations. Also, Applicants note that the layer between the two devices, is actually the lower layer of the upper device; it is not a separate layer as recited in the claimed invention. (See, for example, Figures 11 and 12, elements 16 and 26).

Accordingly, Applicants respectfully request that the rejection over claims 15-20 be withdrawn.

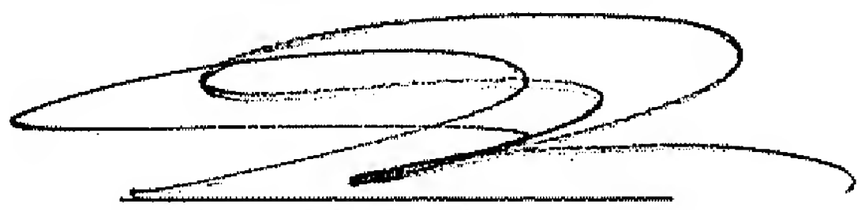
Other Matters

Claims 21-24 are added for the Examiner's consideration. Claims 21-24 are depend from a distinguishable base claim. Accordingly, claims 21-24 should also be allowable.

CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,
Mahmoud A. Mousa



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